In the Claims:

Claims 1 to 11 (Cancelled).

12. (Previously Presented) A system-on-chip (SOC) comprising:

a plurality of circuit blocks, each responsive to a respective local clock signal;

a system clock connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals;

a power control manager connected to said circuit blocks for selectively providing a shutdown signal thereto; and

each circuit block comprising a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgment signal to said power control manager.

13. (Previously Presented) An SOC according to Claim 12, wherein each shutdown circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

14. (Previously Presented) An SOC according to Claim 12, wherein said power control manager is connected to each shutdown circuit through a respective power down request line for providing the shutdown signal thereto, and through a

respective power down acknowledgment line for receiving the shutdown acknowledgment signal therefrom.

15. (Previously Presented) An SOC according to Claim 14, wherein each circuit block further comprises a block logic circuit connected to said shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

16. (Previously Presented) An SOC according to Claim 14, wherein each shutdown circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to said system clock, and an output for providing the respective local clock signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

17. (Previously Presented) An SOC according to Claim 14, wherein said power control manager comprises:

a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals; and

a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals.

18. (Previously Presented) An SOC according to Claim 17, further comprising a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said first and second registers.

19. (Previously Presented) An SOC according to Claim 12, further comprising another system clock connected to selected circuit blocks for providing a system clock signal thereto.

20. (Previously Presented) A system-on-chip (SOC) comprising:

a plurality of circuit blocks;

a system clock connected to said circuit blocks for providing a system clock signal thereto; and

a power control manager connected to said circuit blocks for selectively providing a shutdown signal thereto; and

each circuit block comprising

a block logic circuit having an input for receiving the shutdown signal, and an output for providing a shutdown acknowledgment signal to said power control manager after receiving the shutdown signal, and

a shutdown circuit connected to said block logic circuit for preventing the system clock signal from functioning as a local clock signal after said block logic circuit provides the shutdown acknowledgment signal to said power control manager.

21. (Previously Presented) An SOC according to Claim 20, wherein each shutdown circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

22. (Previously Presented) An SOC according to Claim 20, wherein said power control manager is connected to each shutdown circuit through a respective power down request line for providing the shutdown signal thereto, and through a respective power down acknowledgment line for receiving the shutdown acknowledgment signal therefrom.

23. (Previously Presented) An SOC according to Claim 22, wherein each block logic circuit is connected to said shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

24. (Previously Presented) An SOC according to Claim 22, wherein each shutdown circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to said system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

25. (Previously Presented) An SOC according to Claim 22, wherein said power control manager comprises:

a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals; and

a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals.

26. (Previously Presented) An SOC according to Claim 25, further comprising a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said first and second registers.

27. (Previously Presented) A system-on-chip (SOC) comprising:

a plurality of circuit blocks;

a system clock connected to said circuit blocks for providing a system clock signal thereto;

a power control manager connected to said circuit blocks through a respective power down request line for selectively providing a shutdown signal thereto, and through a respective power down acknowledgment line for receiving a shutdown acknowledgment signal therefrom, said power control manager comprising at least one register for storing data indicating logic states of the shutdown signals and the shutdown acknowledgment signals;

a central processing unit connected to said power

control manager for determining whether each circuit block is in an active state or an idle state by querying said at least one register; and

each circuit block comprising a shutdown circuit for preventing the system clock signal from functioning as a local clock signal after the circuit block receiving the shutdown signal provides the shutdown acknowledgment signal to said power control manager.

28. (Previously Presented) An SOC according to Claim 27, wherein each shutdown circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

29. (Previously Presented) An SOC according to Claim 27, wherein each circuit block further comprises a block logic circuit connected to said shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

30. (Previously Presented) An SOC according to Claim 28, wherein each clock separation circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to said system clock, and an output for providing the local clock

signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

31. (Previously Presented) An SOC according to Claim 27, wherein said at least one register comprises:

a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals; and

a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals.

32. (Previously Presented) A method for powering down circuit blocks within a system-on-chip (SOC) comprising a plurality of circuit blocks, the method comprising:

providing a system clock signal to the circuit blocks for functioning as a respective local clock signal;

selectively providing a shutdown signal to the circuit blocks; and

preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgment signal.

33. (Previously Presented) A method according to Claim 32, further comprising preventing the system clock signal from functioning as the respective local clock signal if the corresponding circuit block receiving the shutdown signal is in an idle state.

34. (Previously Presented) A method according to Claim 32, wherein the SOC comprises a power control manager for providing the shutdown signals, and wherein each circuit block comprises a shutdown circuit connected to the power control manager through a respective power down request line for receiving the shutdown signal therefrom, and through a respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

35. (Previously Presented) A method according to Claim 34, wherein each circuit block further comprises a block logic circuit connected to the shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

36. (Previously Presented) A method according to Claim 34, wherein each shutdown circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to a system clock, and an output for providing the respective local clock signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

37. (Previously Presented) A method according to Claim 34, wherein the power control manager comprises a first register connected to the respective power down request lines

for storing data indicating logic states of the shutdown signals, and a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals.

38. (Previously Presented) A method according to Claim 37, further comprising determining whether each circuit block is in an active state or an idle state by querying the first and second registers.